Notice of Allowability	Application No.	Applicant(s)	
	10/763,733	MCELHENY, PETER JOHN	
	Examiner	Art Unit	
	Phallaka Kik	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed on 5/15/06 and interview conducted on 4/26/2006*.

2. ☒ The allowed claim(s) is/are *1-2,5-7,9-13, wherein claims 3-4,8,14-21 have been cancelled and claims 5-6,7,9-13 have been renumbered as 3-10 respectively*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. This Office Action responds to Applicant's Amendment filed on 5/15/06 and interview conducted on 4/26/2006. Claims 1-2,5-7,9-13 are pending, wherein claims 1-2,5-7 have been amended and claims 3-4,8,14-21 have been cancelled. Claims 1-2,5-7,9-13 have been examined and are allowed.

Allowable Subject Matter

2. **Claims 1-2,5-7,9-13** are allowed.

3. The following is an examiner's statement of reasons for allowance:

As per **claims 1-2,5-7,9-13**, the independent claims 1 and 7, from which the respective claims depend, recite the methods for using a logic design system to minimize power consumption in a programmable logic device, comprising the inventive steps of generating/producing configuration data for the programmable logic device which takes into account power consumption due to gate leakage effects, wherein signals are routed on the programmable logic device to positions within the stacks of transistors in the programmable logic device, based on the amounts that the signals are expected to be high or low, including (as per claims 7,9-13) ensuring that signals that are more likely to be high are routed to the transistor gates of the transistors higher in the stacks and that signals that are less likely to be high are routed to the transistor gates of the transistors lower in the stacks, as claimed, which the prior arts made of record failed to teach or suggest, wherein as pointed out by Applicant's Representative in the interview conducted on 4/26/2006, **Rafik S. Guindi et al.** ("Design Techniques for Gate-Leakage Reduction in CMOS Circuits", 2003 IEEE, pp. 61-65, especially pages

63-65) fails to teach or suggest how to ensure the routing of the signals to be at certain positions within the stacks of transistors in the programmable logic device based on the likelihood or expectation of the signals to be high or low, as claimed. Other prior arts made of record similarly failed to teach or suggest the inventive steps as claimed. Accordingly, the claimed invention is novel and un-obvious over the prior arts made of record.

Conclusion

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Monday-Thursday, 8:30AM-7PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

571-273-8300

Phallaka Kik
U.S. Patent Examiner
May 23, 2006